Development of Front–End Electronics for Beam Condition Monitor at CMS

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Outline

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3 Architecture
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5 Calibration Circuit
6 Layout and PCB
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Motivation

Events statistics

Both peaking time and pulse duration not sufficient for 25 ns beam operation

MIP signal

Overdrive signal
The Design Goals

- BCM1F system will be used for luminosity and beam background measurements
- Expected luminosity between LHC long shutdowns $> 150 \text{ fb}^{-1}$ – rad-hard design needed
- 2 – 5 pF detector capacitance range
- $\sim 15 \text{ fC}$ linearity range
- $\sim 50 \text{ mV/fC}$ of charge gain
- Equivalent Noise Charge $< 1 \text{ke}^-$
- Quasi-Gaussian shaping with $T_p$ and FWHM $< 10 \text{ ns}$
- Fast baseline recovery after overdrive detector signal
- Default polarity of the detector – electron signal.
- Hi-performance output buffer needed – 100 $\Omega$ & 10pF load
Architecture

Schematic diagram of FE channel

- Preampilier
- Shaper
- Amplifier and single-to-differential converter with output buffer
- Linear Laser Driver
Preamplifier

- IBM CMOS8RF 130nm technology
- 2.5 V power supply (high voltage enabled design)
- 85 dB of DC gain with \(~ 80^\circ\) phase margin
- \(~ 1.6 \text{ GHz} \) GBP (2.4 GHZ w/o comp.)
- \(~ 7.5 \text{ mS} \) input transistor \(g_m\)
- \(~ 350 \mu A \) current consumption (\(~ 870 \mu W\))

Output buffer

- Class AB Push–Pull operation
- \(~ 9\text{mA} \) output current capability (ltd by safety diodes)
- \(~ 10 \text{ mW} \) of power consumption
- \(~ 240 \text{ MHz} \) GBP
Simulation results

Linearity

Linearity and Gain

Charge gain \((C_{\text{det}} = 5\text{pF}) = 57.4 \text{ mV/fC}\)
Simulation results
Time response

Front–End response on MIP signal

Peaking Time = 9.2 (ns)
FWHM = 7.1 (ns)
Simulation results
Time response

Distinguishability of MIPs with 12.5 ns interval

Output Voltage (mV) vs Time (ns)
Simulation results

Time response

Front-End response on large signals

- $Q_{in} = 30$ (fC)
- $Q_{in} = 100$ (fC)
- $Q_{in} = 250$ (fC)
- $Q_{in} = 500$ (fC)
Simulation results
FE parameters dependency to detector capacitance

Peaking time variation

FWHM variation
**Simulation results**
FE parameters dependency to detector capacitance

**Equivalent Noise Charge**

ENC Slope = 69.5 \( (\text{e}^-/\text{pF}) \)

**Power Supply Rejection Ratio**

The PSRR at high frequencies degraded to about -10 dB due to use of safety clamping diodes (should not be a problem for a system with a few number of channels)
Simplified Scheme

BandGap Reference

\[ V_{\text{high}} \]

\[ V_{\text{low}} \]

\[ C_{\text{test}} \]

Select

LVDS

Strobe

Specification

- common calibration pulse for all channels
- 2 levels of charge (1 bit for selection)
- Differential driver (LVDS) for Strobe signal
Chip floorplan – 5.6 × 2 mm²
Layout and PCB
Concept for the Upgrade

- Carbon fiber carriage,
- C-Shaped PCB to hold BCM1F diamonds & amplifiers & BCM1L diamond modules.
- Laser diodes on carriage arm (Radius 120 mm)
- Planning new cabling for up to 12 1F "diamonds"/quadrant + 2 1L diamonds.
Conclusion

The FEE are done on schematic level – layout in progress (submission in 19.02.2013)

Use of 2.5 V supply for FEE core allows to meet the specification in terms of $T_P$ (9 ns) and FWHM (7 ns)

Frontend meets the specification: ENC $<800$ e$^-$, $K_q \sim 57$ mV/fC, input range $\sim 15$ fC (10 fC – linear)

Acknowledgements

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Vladimir Ryjov and Anne Dabrowski

DESY:
Wolfgang Lohmann and Wolfgang Lange
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