Development of Front–End Electronics for Beam Condition Monitor at CMS

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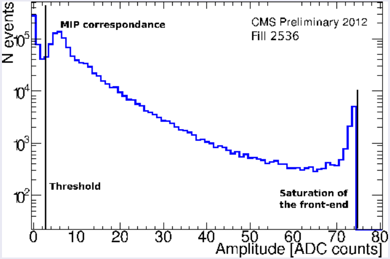
Outline

Motivation

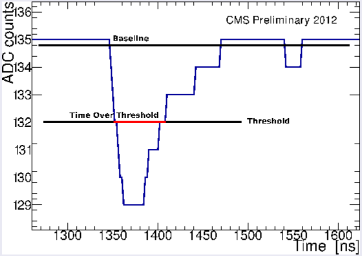
present system

Events statistics

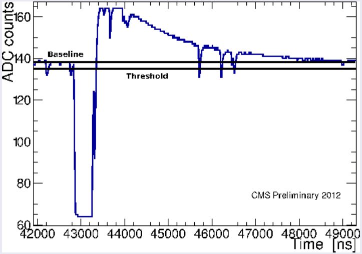


Both peaking time and pulse duration not sufficient for 25 ns beam operation

MIP signal



Overdrive signal



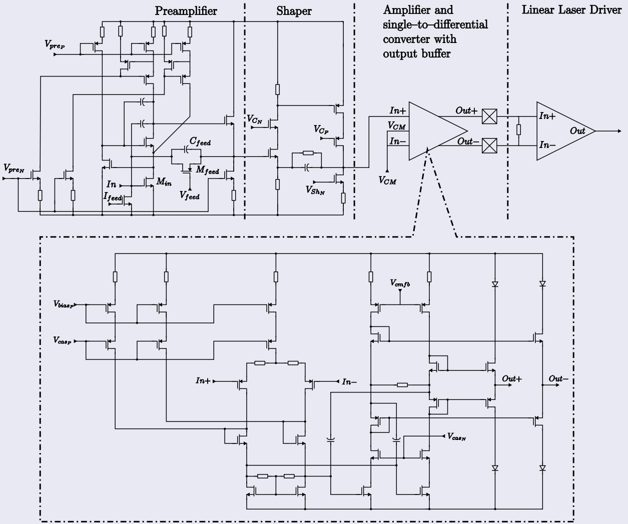
Specification

The Design Goals

- BCM1F system will be used for luminosity and beam background measurements
- Expected luminosity between LHC long shutdowns $> 150\ ^{1}/_{fb}$ – rad–hard design needed
- 2 – 5 pF detector capacitance range
- $\sim$ 15 fC linearity range
- $\sim$50 mV/fC of charge gain
- Equivalent Noise Charge $< 1\mathrm{ke}^{-}$
- Quasi–Gaussian shaping with $\mathrm{T_P}$ and FWHM $<$ 10 ns
- Fast baseline recovery after overdrive detector signal
- Default polarity of the detector – electron signal.
- Hi-performance output buffer needed – 100 Ω & 10pF load

Architecture

Schematic diagram of FE channel



Architecture

Front–End specification

Preamplifier

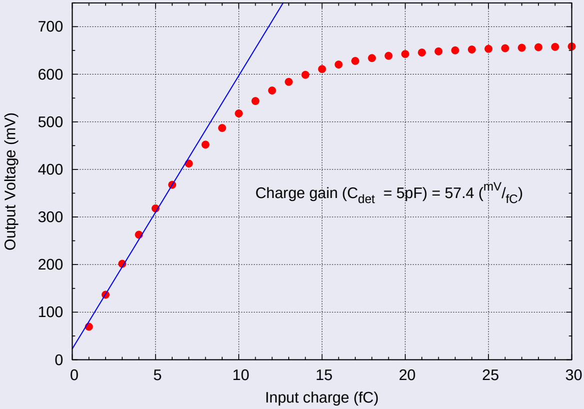
- IBM CMOS8RF 130nm technology
- 2.5 V power supply (high voltage enabled design)
- 85 dB of DC gain with $\sim 80^o$ phase margin
- $\sim$ 1.6 GHz GBP (2.4 GHZ w/o comp.)
- $\sim$ 7.5 mS input transistor g_m
- $\sim$350 μA current consumption ($\sim$ 870 μW)

Output buffer

- Class AB Push–Pull operation
- $\sim$ 9mA output current capability (ltd by safety diodes)
- $\sim$ 10 mW of power consumption
- $\sim$ 240 MHz GBP

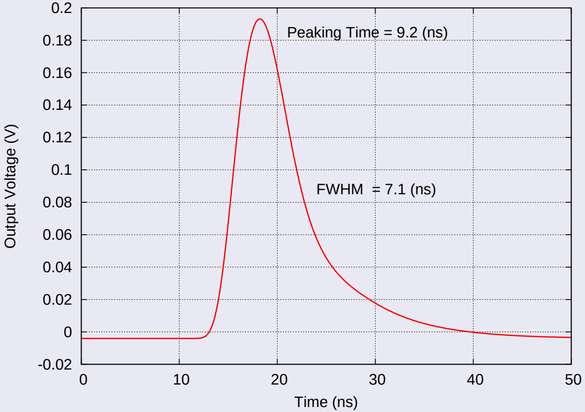
Simulation results
Linearity

Linearity and Gain



Simulation results
Time response

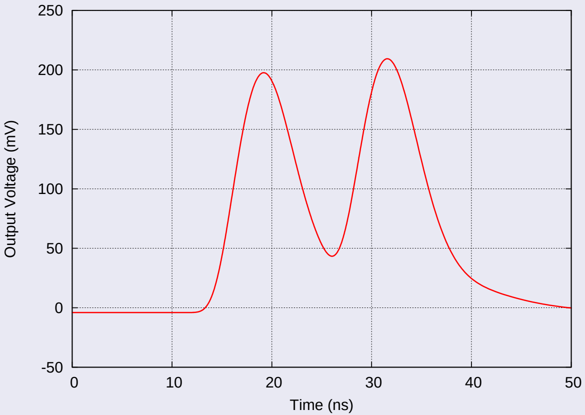
Front–End response on MIP signal



Simulation results

Time response

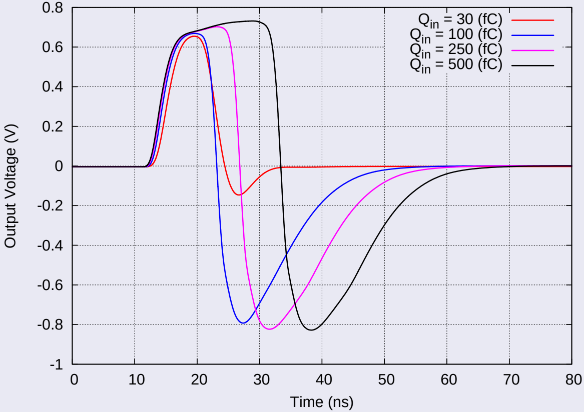
Distinguishability of MIPs with 12.5 ns interval



Simulation results

Time response

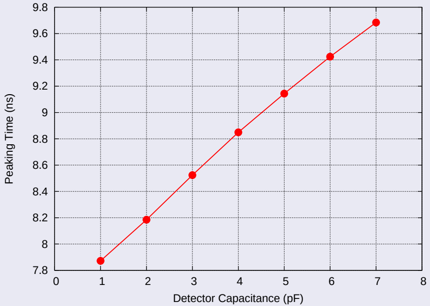
Front–End response on large signals



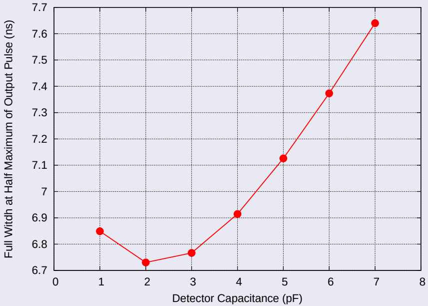
Simulation results

FE parameters dependency to detector capacitance

Peaking time variation



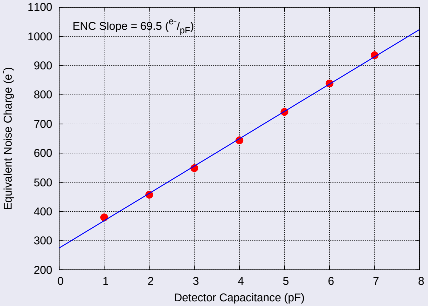
FWHM variation



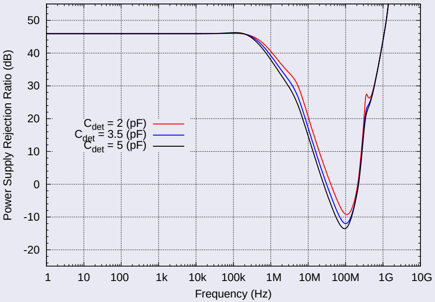
Simulation results

FE parameters dependency to detector capacitance

Equivalent Noise Charge



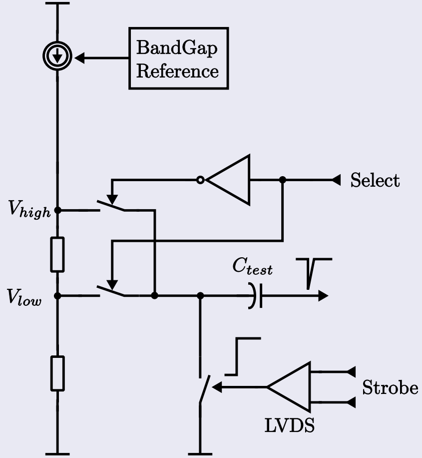
Power Supply Rejection Ratio



The PSRR at high frequencies degraded to about -10 dB due to use of safety clamping diodes (should not be a problem for a system with a few number of channels)

Calibration Circuit

Simplified Scheme

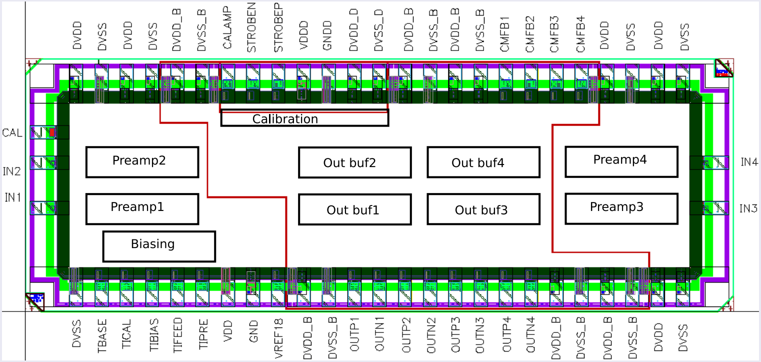


Specification

- common calibration pulse for all channels
- 2 levels of charge (1 bit for selection)
- Differential driver (LVDS) for Strobe signal

Layout and PCB

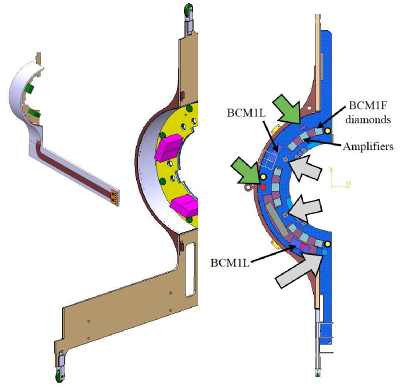
Chip floorplan – $5.6 \times 2\ mm^2$



Layout and PCB

Concept for the Upgrade

PCB design



- Carbon fiber carriage,
- C-Shaped PCB to hold BCM1F diamonds & amplifiers & BCM1L diamond modules.
- Laser diodes on carriage arm (Radius 120 mm)
- Planning new cabling for up to 12 1F "diamonds"/quadrant + 2 1L diamonds.

Conclusion

Colnclusion

- The FEE are done on schematic level – layout in progress (submission in 19.02.2013)
- Use of 2.5 V supply for FEE core allows to meet the specification in terms of T_P (9 ns) and FWHM (7 ns)
- Frontend meets the specification: ENC <800 e^-, K_q ~57 mV/fC, input range ~ 15 fC (10 fC – linear)

Acknowledgements

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- DESY:
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